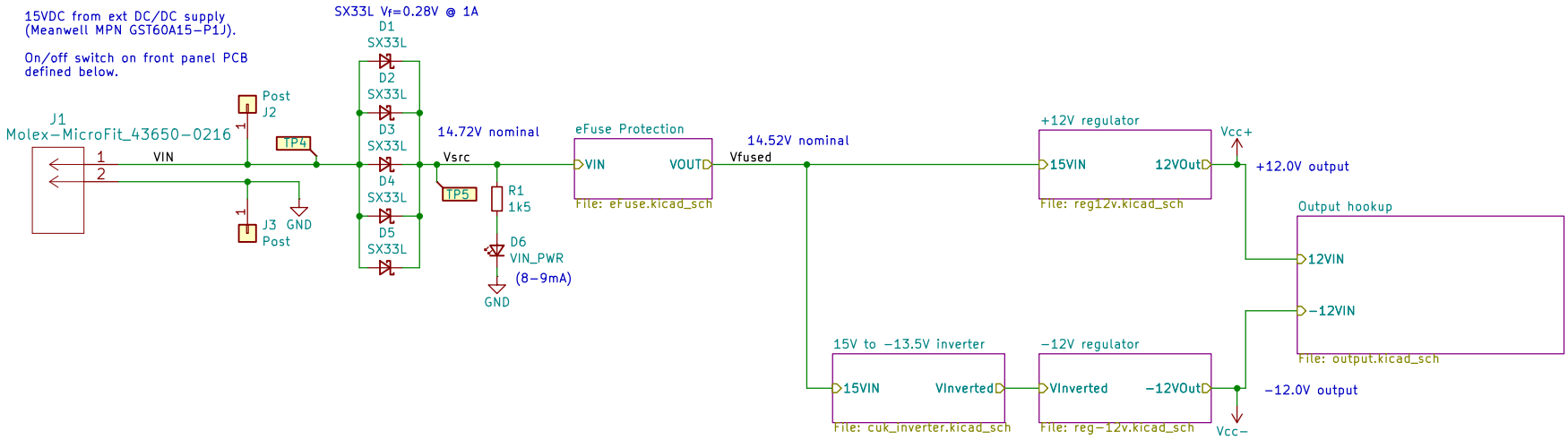
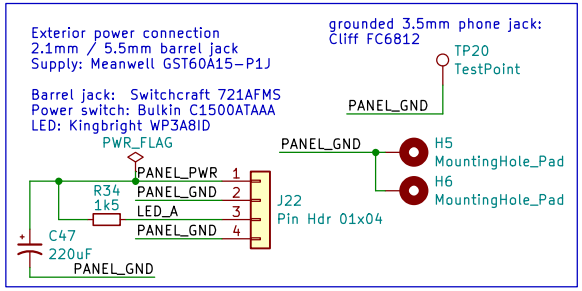
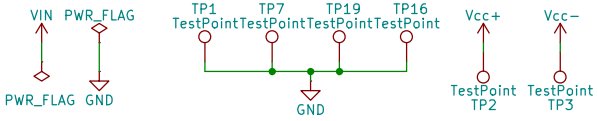
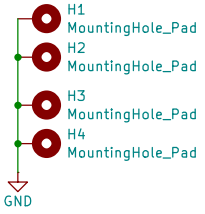








ERRATA

REV 2:
- Q6 oriented backward on PCB (fixed in r2.1)
- RESET (SW1) falling edge can trigger TPS2421 $\overline{\text{FLT}}$
  (Too much inrush? TPS2421 does not re-enter SOA protect mode?
  Are the supply soft starts and inverter delays inactive on reset?
  Filter inductors causing V_{OUT} / V_{IN} disagreement?)

NOTES

Assembling 3314J trimpots connected to GND on 2oz plane
via hot air caused degradation of trimpot linearity.
Hand-assemble with iron, try hot air + preheating hot plate,
or use a more durable trimpot in the future.

TODO: Consider replacing RV1 and RV3 with 5-turn 3214W-1-102E
to make it easier to dial in voltage rails more precisely.

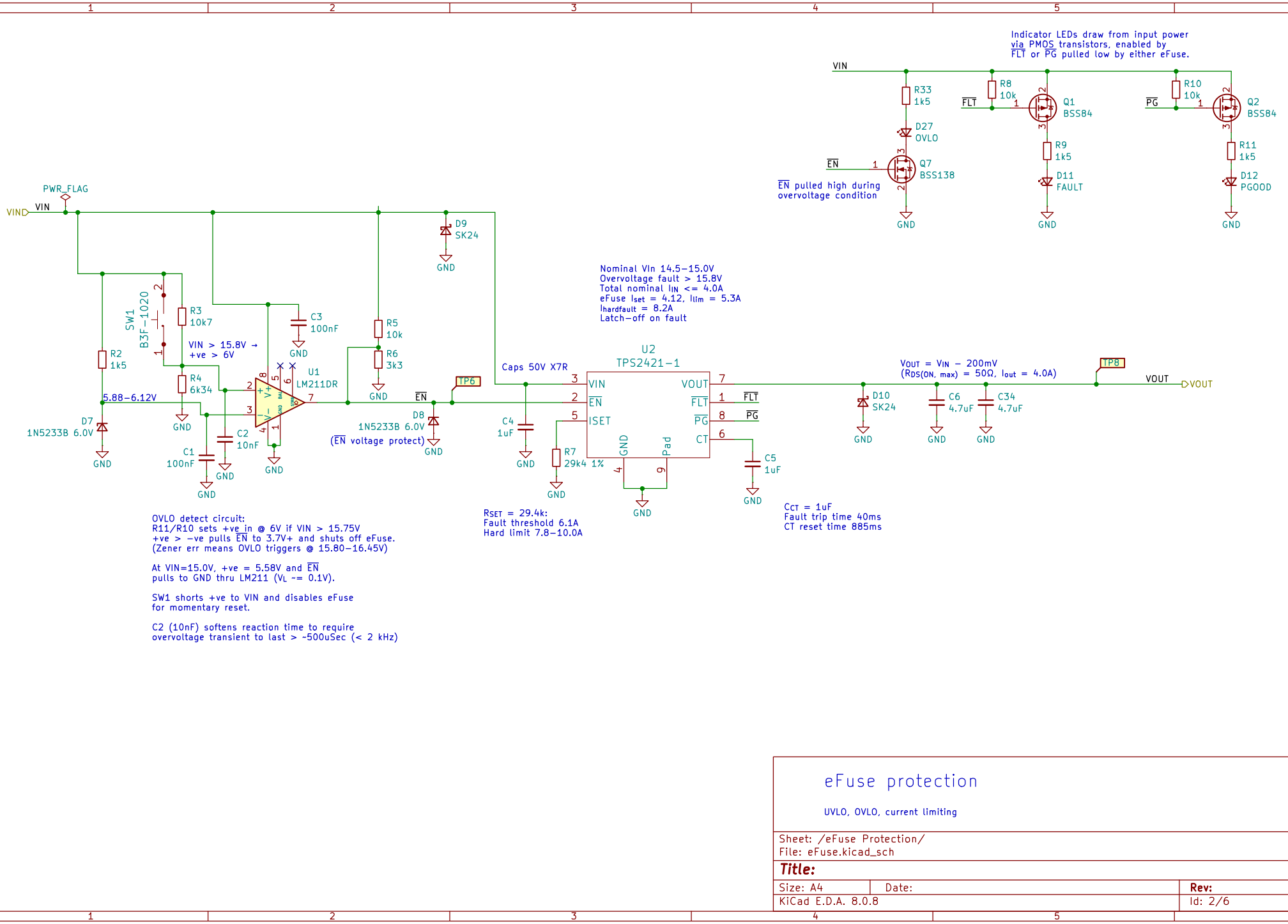
GS-101-PWR rev 2.1

Input: ±15V 4A (60W) DC
Output: Linear regulated ±12VDC, 48W (3A @ +12V, 1A @ -12V)

Sheet: /
File: GS-101-PWR v2.kicad_sch

Title:

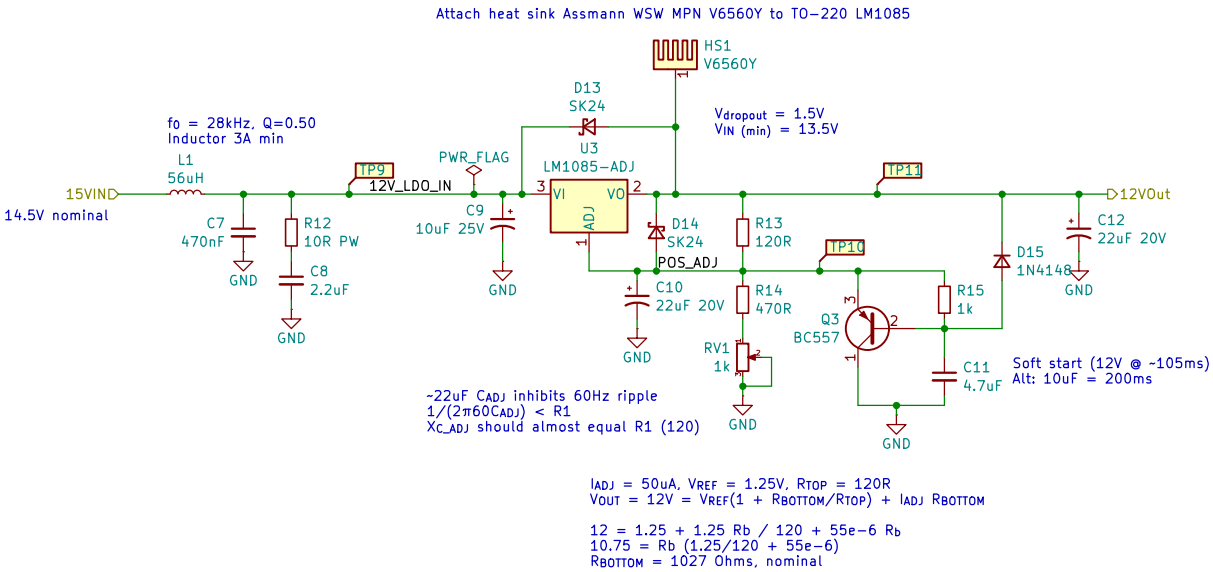
Size: A4	Date:	**Rev:** 2.1
KiCad E.D.A. 8.0.8		Id: 1/6



eFuse protection

UVLO, OVLO, current limiting

Sheet: /eFuse Protection/		
File: eFuse.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 2/6

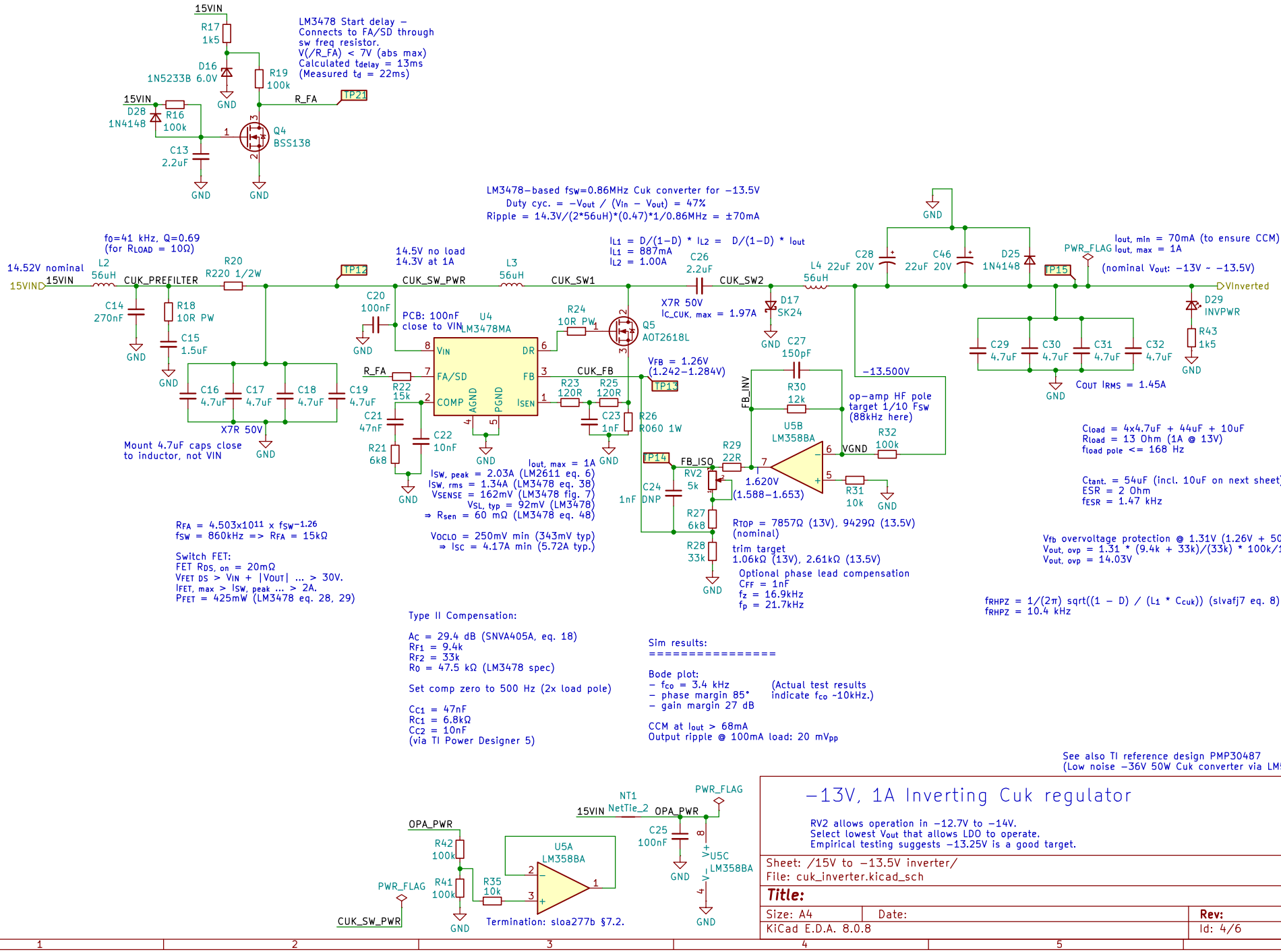


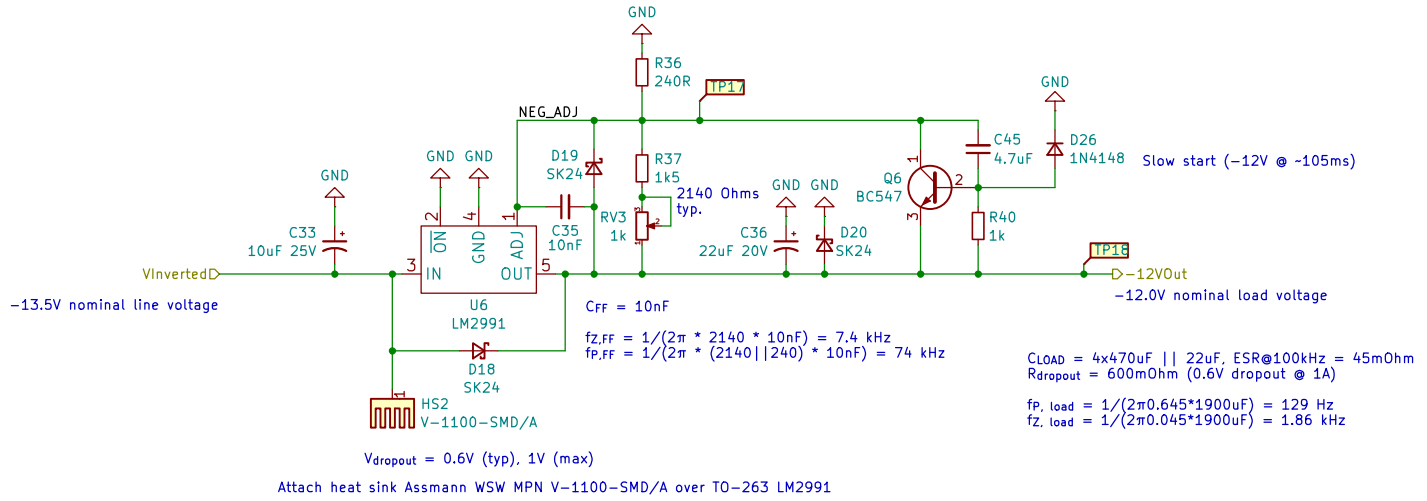
+12V regulator, 3A

Sheet: /+12V regulator/
File: reg12v.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 3/6


15VIN
R17 1k5
D16 1N5233B 6.0V
R19 100k
GND
R_FA
TP21
LM3478 Start delay –
Connects to FA/SD through
sw freq resistor.
V(/R_FA) < 7V (abs max)
Calculated tdelay = 13ms
(Measured td = 22ms)
D28 1N4148
R16 100k
Q4 BSS138
C13 2.2uF
LM3478–based fSW=0.86MHz Cuk converter for –13.5V
Duty cyc. = –Vout / (Vin – Vout) = 47%
Ripple = 14.3V/(2*56uH)*(0.47)*1/0.86MHz = ±70mA
fo=41 kHz, Q=0.69
(for RLOAD = 10Ω)
14.52V nominal
15VIN
L2 56uH
CUK_PREFILTER
R20 R220 1/2W
C14 270nF
R18 10R PW
C15 1.5uF
C16 4.7uF
C17 4.7uF
C18 4.7uF
C19 4.7uF
X7R 50V
Mount 4.7uF caps close
to inductor, not VIN
TP12
14.5V no load
14.3V at 1A
CUK_SW_PWR
L3 56uH
CUK_SW1
C20 100nF
PCB: 100nF
close to VIN
U4 LM3478MA
VIN
FA/SD
COMP
AGND
PGND
DR
FB
ISEN
R24 10R PW
Q5 AOT2618L
R_FA
R22 15k
C21 47nF
R21 6k8
C22 10nF
R23 120R
R25 120R
C23 1nF
R26 R060 1W
CUK_FB
TP13
IL1 = D/(1–D) * IL2 = D/(1–D) * Iout
IL1 = 887mA
IL2 = 1.00A
C26 2.2uF
X7R 50V
IC_CUK, max = 1.97A
CUK_SW2
D17 SK24
C27 150pF
VFB = 1.26V
(1.242–1.284V)
ISW, peak = 2.03A (LM2611 eq. 6)
ISW, rms = 1.34A (LM3478 eq. 38)
VSENSE = 162mV (LM3478 fig. 7)
VSL, typ = 92mV (LM3478)
⇒ Rsen = 60 mΩ (LM3478 eq. 48)
VOCLO = 250mV min (343mV typ)
⇒ ISC = 4.17A min (5.72A typ.)
Iout, max = 1A
TP14
FB_ISO
RV2 5k
C24 DNP 1nF
R27 6k8
R28 33k
RTOP = 7857Ω (13V), 9429Ω (13.5V)
(nominal)
trim target
1.06kΩ (13V), 2.61kΩ (13.5V)
Optional phase lead compensation
CFF = 1nF
fz = 16.9kHz
fp = 21.7kHz
FB_INV
R30 12k
U5B LM358BA
R29 22R
R32 100k
R31 10k
VGND
1.620V
(1.588–1.653)
–13.500V
op–amp HF pole
target 1/10 Fsw
(88kHz here)
L4 22uF 20V 56uH
C28 22uF 20V
C46 22uF 20V
D25 1N4148
PWR_FLAG
TP15
Iout, min = 70mA (to ensure CCM)
Iout, max = 1A
(nominal Vout: –13V ~ –13.5V)
VInverted
D29 INVPWR
R43 1k5
C29 4.7uF
C30 4.7uF
C31 4.7uF
C32 4.7uF
COUT IRMS = 1.45A
Cload = 4x4.7uF + 44uF + 10uF
Rload = 13 Ohm (1A @ 13V)
fload pole <= 168 Hz
Ctant. = 54uF (incl. 10uF on next sheet)
ESR = 2 Ohm
fESR = 1.47 kHz
Vfb overvoltage protection @ 1.31V (1.26V + 50mV)
Vout, ovp = 1.31 * (9.4k + 33k)/(33k) * 100k/12k
Vout, ovp = 14.03V
fRHPZ = 1/(2π) sqrt((1 – D) / (L1 * CCuk)) (slvafj7 eq. 8)
fRHPZ = 10.4 kHz
RFA = 4.503x10^11 x fSW^–1.26
fSW = 860kHz => RFA = 15kΩ
Switch FET:
FET RDS, on = 20mΩ
VFET DS > VIN + |VOUT| ... > 30V.
IFET, max > ISW, peak ... > 2A.
PFET = 425mW (LM3478 eq. 28, 29)
Type II Compensation:
AC = 29.4 dB (SNVA405A, eq. 18)
RF1 = 9.4k
RF2 = 33k
RO = 47.5 kΩ (LM3478 spec)
Set comp zero to 500 Hz (2x load pole)
CC1 = 47nF
RC1 = 6.8kΩ
CC2 = 10nF
(via TI Power Designer 5)
Sim results:
==========
Bode plot:
– fco = 3.4 kHz
– phase margin 85°
– gain margin 27 dB
(Actual test results
indicate fco ~10kHz.)
CCM at Iout > 68mA
Output ripple @ 100mA load: 20 mVpp
See also TI reference design PMP30487
(Low noise –36V 50W Cuk converter via LM5022)
NT1 NetTie_2
15VIN
OPA_PWR
PWR_FLAG
C25 100nF
U5C LM358BA
R42 100k
R41 100k
R35 10k
U5A LM358BA
CUK_SW_PWR
Termination: sloa277b §7.2.
–13V, 1A Inverting Cuk regulator
RV2 allows operation in –12.7V to –14V.
Select lowest Vout that allows LDO to operate.
Empirical testing suggests –13.25V is a good target.
Sheet: /15V to –13.5V inverter/
File: cuk_inverter.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.8
Id: 4/6



−12V regulator, 1A

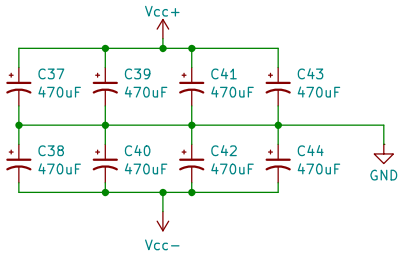
Sheet: /−12V regulator/
File: reg−12v.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 5/6

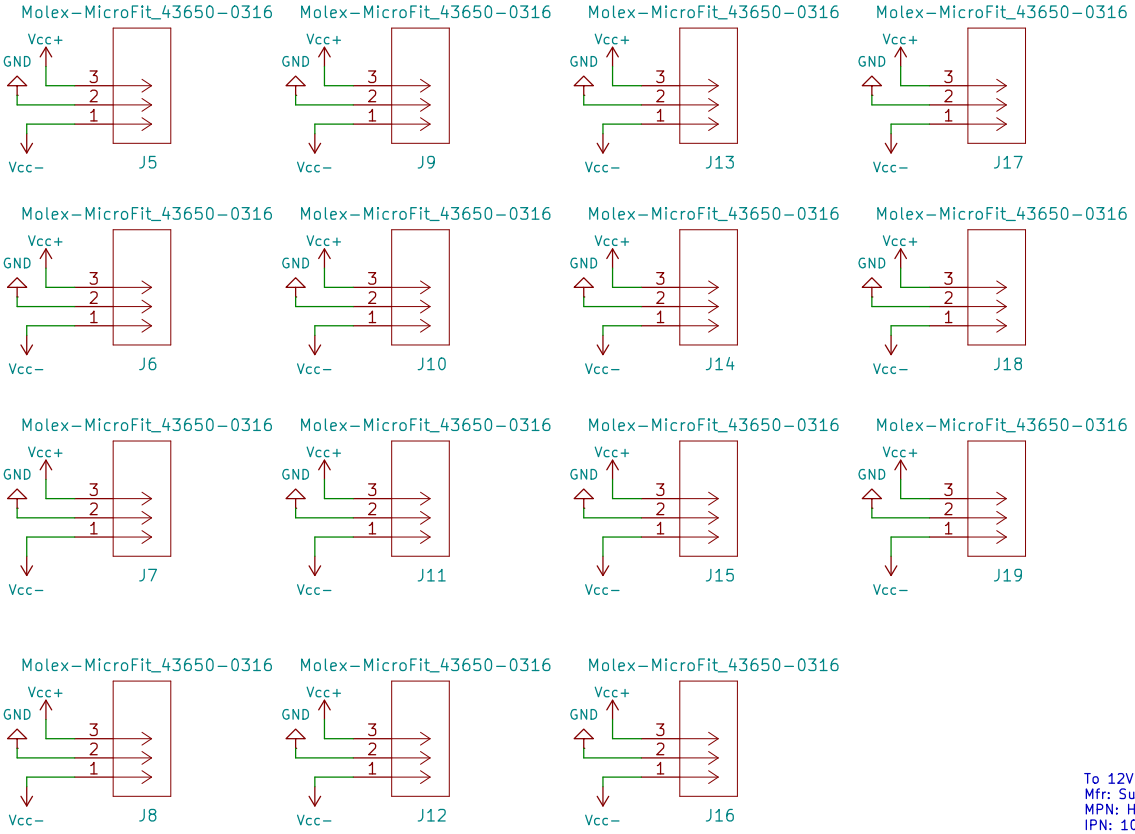
12VIN
Vcc+
-12VIN
Vcc-

Module-level bulk decoupling.
Electrolytic caps 25V min.

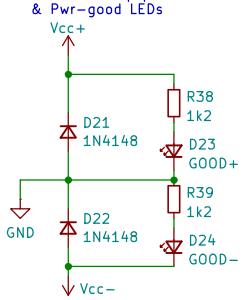


Power distributed to other PCBs/modules
thru Molex MicroFit 3.0 3-pin c'tor
MPN 043650-0316

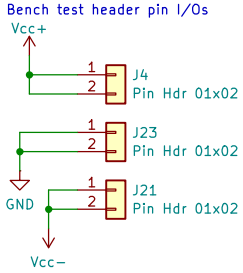
Mates with Molex F--F 3-pin cable assy
MPN 2147502032 (300mm)
or MPN 2147502033 (600mm)



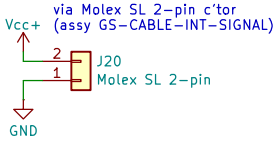
Anti-latch-up protection
& Pwr-good LEDs



Bench test header pin I/Os



To 12V 22mA case fan.
Mfr: Sunon
MPN: HA60251V4-1000U-A99
IPN: 100534
via Molex SL 2-pin c'tor
(assy GS-CABLE-INT-SIGNAL)



Sheet: /Output hookup/
File: output.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 6/6